L Number	Hits	Search Text	DB	Time stamp
1	118096	wir$4 near4 layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 18:31
2	31246	(wir$4 near4 layer) and arrang$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 18:31
3	19549	((wir$4 near4 layer) and arrang$4) and contact	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 18:32
4	2341	(((wir$4 near4 layer) and arrang$4) and contact) and tool	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 18:32
5	84	(((wir$4 near4 layer) and arrang$4) and contact) and (layout near4 tool)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 18:37
6	80	((((wir$4 near4 layer) and arrang$4) and contact) and (layout near4 tool)) and function$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 18:37
8	123	automatic near4 layout near4 tool	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:39
9	21	(automatic near4 layout near4 tool) and wir$4 and exten$7 and contact and layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:44
10	34	(automatic near4 layout near4 tool) and (electrical$4 same connect$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:45
11	23	((automatic near4 layout near4 tool) and (electrical$4 same connect$4)) and function$4 and chip and arrang$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:46
7	67	(((((wir$4 near4 layer) and arrang$4) and contact) and (layout near4 tool)) and function$4) and exten$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:52
12	67	((((((wir$4 near4 layer) and arrang$4) and contact) and (layout near4 tool)) and function$4) and exten$6) and connect$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:53
13	12	(automatic near4 layout near4 tool) and (exten$7 same arrang$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:54
15	8	((automatic near4 layout near4 tool) and (exten$7 same arrang$4)) and wir$4 and connect and function$4 and layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:55

14	61	((((((wir$4 near4 layer) and arrang$4) and contact) and (layout near4 tool)) and function$4) and exten$6) and connect$4) and wir$4 and connect and function$4 and layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/02 19:56

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040065907 A1	20040408	20	Semiconductor device, designing method thereof, and recording medium storing semiconductor designing program	257/211
2	US 20040056280 A1	20040325	46	Semiconductor device and a method of manufacturing the same	257/208
3	US 20040053429 A1	20040318	119	Method for identifying semiconductor integrated circuit device, method for manufacturing semiconductor integrated circuit device, semiconductor integrated circuit device and semiconductor chip	438/17
4	US 20030237072 A1	20031225	13	Systems and methods for generating an artwork representation according to a circuit fabrication process	716/19
5	US 20030237069 A1	20031225	40	EFFICIENT LAYOUT STRATEGY FOR AUTOMATED DESIGN LAYOUT TOOLS	716/8
6	US 20030209727 A1	20031113	30	Semiconductor integrated circuit	257/200
7	US 20030167452 A1	20030904	31	Design system of semiconductor integrated circuit element, program, program product, design method of semiconductor integrated circuit element, and semiconductor integrated circuit element	716/8
8	US 20030140327 A1	20030724	14	Method of designing power vias in an IC layout	716/12
9	US 20030115568 A1	20030619	24	Method of designing, fabricating, testing and interconnecting an IC to external circuit nodes	716/15

	Document ID	Issue Date	Pages	Title	Current OR
10	US 20030084417 A1	20030501	14	Method of designing conductive pattern layout of LSI	716/10
11	US 20030023946 A1	20030130	10	Standard cell library generation using merged power method	716/17
12	US 20020171449 A1	20021121	38	Test system and manufacturing of semiconductor device	324/765
13	US 20020140456 A1	20021003	33	Semiconductor integrated circuit device	326/81
14	US 20020113234 A1	20020822	38	Method and system for inspecting electronic circuit pattern	257/48
15	US 20020101759 A1	20020801	16	SHARED GROUND SRAM CELL	365/154
16	US 20020093036 A1	20020718	13	Integrated circuit power and ground routing	257/208
17	US 20020072135 A1	20020613	17	Manufacturing method of semiconductor integrated circuit device	438/15
18	US 20020009834 A1	20020124	74	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	438/142
19	US 20010039644 A1	20011108	41	Chip carrier layer count calculator	716/11
20	US 20010014051 A1	20010816	75	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	365/230.03
21	US 20010000427 A1	20010426	24	Method of incorporating interconnect systems into an integrated circuit process flow	333/33
22	US 6772406 B1	20040803	13	Method for making large-scale ASIC using pre-engineered long distance routing structure	716/12

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23	US 6753611 B1	20040622	19	Semiconductor device, designing method thereof, and recording medium storing semiconductor designing program	257/774
24	US 6753253 B1	20040622	326	Method of making wiring and logic corrections on a semiconductor device by use of focused ion beams	438/676
25	US 6728113 B1	20040427	67	Method and apparatus for non-conductively interconnecting integrated circuits	361/760
26	US 6727723 B2	20040427	36	Test system and manufacturing of semiconductor device	324/765
27	US 6708319 B2	20040316	17	Manufacturing method of semiconductor integrated circuit device	716/5
28	US 6701509 B2	20040302	13	Integrated circuit power and ground routing	716/13
29	US 6609240 B2	20030819	13	Method of designing conductive pattern layout of LSI	716/10
30	US 6609236 B2	20030819	71	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	716/8
31	US 6601227 B1	20030729	13	Method for making large-scale ASIC using pre-engineered long distance routing structure	716/12

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32	US 6574780 B2	20030603	40	Method and system for electronically modeling and estimating characteristics of a multi-layer integrated circuit chip carrier	716/4
33	US 6539531 B2	20030325	23	Method of designing, fabricating, testing and interconnecting an IC to external circuit nodes	716/15
34	US 6453454 B1	20020917	11	Automatic engineering change order methodology	716/11
35	US 6426890 B1	20020730	16	Shared ground SRAM cell	365/154
36	US 6407434 B1	20020618	136	Hexagonal architecture	257/401
37	US 6404232 B1	20020611	31	Semiconductor integrated circuit device	326/81
38	US 6400173 B1	20020604	36	Test system and manufacturing of semiconductor device	324/765
39	US 6388332 B1	20020514	13	Integrated circuit power and ground routing	257/774
40	US 6378115 B1	20020423	32	LSI manufacturing method and recording medium for storing layout software	716/7

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41	US 6335898 B1	20020101	72	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	365/230.03
42	US 6312980 B1	20011106	134	Programmable triangular shaped device having variable gain	438/197
43	US 6307162 B1	20011023	10	Integrated circuit wiring	174/262
44	US 6246629 B1	20010612	70	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	365/230.03
45	US 6209123 B1	20010327	114	Methods of placing transistors in a circuit layout and semiconductor device with automatically placed transistors	716/14
46	US 6140686 A	20001031	32	Semiconductor integrated circuit device	257/369
47	US 6097663 A	20000801	70	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	365/230.03

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48	US 6097073 A	20000801	138	Triangular semiconductor or gate	257/401
49	US 6075934 A	20000613	15	Method for optimizing contact pin placement in an integrated circuit	716/10
50	US 6069834 A	20000530	71	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	365/230.03
51	US 6006024 A	19991221	112	Method of routing an integrated circuit	716/12
52	US 5995439 A	19991130	70	Semiconductor IC device having a memory and a logic circuit implemented with a single chip	365/230.03
53	US 5987086 A	19991116	113	Automatic layout standard cell routing	716/1
54	US 5984510 A	19991116	113	Automatic synthesis of standard cell layouts	716/2
55	US 5973376 A	19991026	136	Architecture having diamond shaped or parallelogram shaped cells	257/401
56	US 5889329 A	19990330	139	Tri-directional interconnect architecture for SRAM	257/758

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57	US 5872380 A	19990216	136	Hexagonal sense cell architecture	257/369
58	US 5864165 A	19990126	141	Triangular semiconductor NAND gate	257/401
59	US 5834821 A	19981110	140	Triangular semiconductor "AND" gate device	257/401
60	US 5822214 A	19981013	135	CAD for hexagonal architecture	716/10

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61	US 5811863 A	19980922	136	Transistors having dynamically adjustable characteristics	257/401
62	US 5808330 A	19980915	136	Polydirectional non-orthoginal three layer interconnect architecture	257/208
63	US 5801422 A	19980901	139	Hexagonal SRAM architecture	257/369
64	US 5789770 A	19980804	136	Hexagonal architecture with triangular shaped cells	257/206

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65	US 5777360 A	19980707	137	Hexagonal field programmable gate array architecture	257/315
66	US 5742086 A	19980421	136	Hexagonal DRAM array	257/300
67	US 5629838 A	19970513	68	Apparatus for non-conductively interconnecting integrated circuits using half capacitors	361/782